GaNPower International Inc.

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230 -3410 LOUGHEED HWY
VANCOUVER, BC, V5M 2A4 CANADA

GPIXU30SB5L

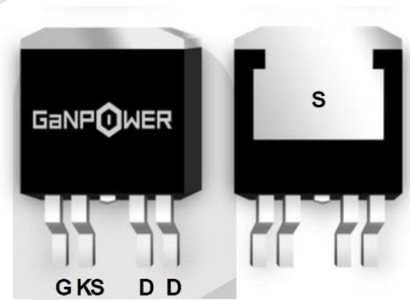
N-channel 1200V 30A GaN Power HEMT in TO263-5L Package

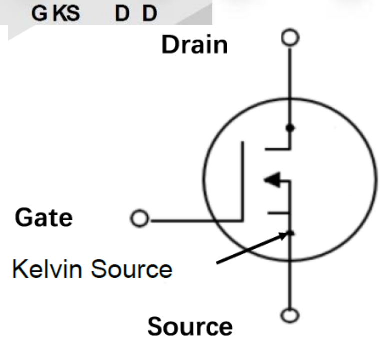
Datasheet version 5.3

Features

BV_{dss}	R_{dson}	I_{ds}	Q_g
1200 V	70 mΩ	30 A	11.2 nC

- Ultra-low R_{DS}(on)
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Outstanding switching performance
- Low Profile





Applications

- Switching Power Applications
- Server and Telecom Power Application
- EV OBC and DC-DC Converters
- UPS, Inverters, PV

Description

These devices are N-channel 1200 V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology. The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.

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Device Characteristics

Static Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$V_{gs(TH)}$	Gate threshold voltage	$V_{ds}=V_{gs}$, I_d=3.5mA (T_J=25 °C)	1.01	1.3	1.7	V
			$V_{ds}=V_{gs}$, I_d=3.5mA (T_J=150 °C)		1.04		V
2	BV_{dss}	Drain-Source breakdown voltage	V_{gs}=0V, I_d < 20 µA (T_J=25 °C)		1200		V
3	I_{dss}	Zero gate voltage drain leakage current	V_{gs}=0V, V_{ds}=1200V T_J = 25℃		0.5	20	µA
			V_{gs}=0V V_{ds}=1200V T_J = 150℃		130		µA
4	I_{gss}	Gate-Source Leakage	V_{gs} = 6V, V_{ds} = 0V		65	150	µA
5	R_{dson}	drain-source on resistance	V_{gs}=6V, I_d=7.5A T_J = 25℃		70	90	mΩ
			V_{gs}=6V, I_d=7.5A T_J = 150℃		147		mΩ
6	V_{sd}	Reverse conduction voltage	I_{sd}=1A, V_{gs}=0V	1.65	1.95	2.30	V
7	R_g	Gate resistance	f=25Mhz Open drain		1.5		Ω
Dynamic Parameters				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	C_{ISS}	Input capacitance	V_{gs} = 0V V_{ds} = 800V F = 1MHz		223		pf
2	C_{OSS}	Output capacitance			79		pf
3	C_{RSS}	Reverse transfer capacitance			3.2		pf
4	$C_{O(er)}$	Effective output capacitance, energy related	V_{ds} = 0 - 800V		98		pf
5	Q_g	Gate charge	V_{ds} = 400V I_d = 9A V_{gs} = 6V		11.2		nC
6	Q_{gs}	Gate to source charge			2.7		nC
7	Q_{gd}	Gate to drain charge			5.7		nC
8	Q_{OSS}	Output Charge	V_{ds} = 0 - 800V		105		nC
9	Q_{rr}	Reverse recovery charge			0		nC

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Switching Performance				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$t_{d(on)}$	Turn-on delay time	V_{ds}=800V I_d=7A R_g=22/2Ω V_{gs}=-3/6V		19		ns
2	t_r	Rise time			20		ns
3	$t_{d(off)}$	Turn-off delay time			17		ns
4	t_f	Fall time			40		ns

Absolute Max. Ratings

	Symbols	Parameters	Value	Unit
1	$V_{DS\text{-}max}$	Breakdown voltage transient @ T_{case}=25°C	1400	V
2	$V_{DS\text{-}max}$	Breakdown voltage transient @ T_{case}=125°C	1250	V
3	$V_{GS\text{-}max}$	Gate to source max. voltage @ T_{case}=25°C	-12 to +7	V
4	$I_{ds\text{-}max}$	Drain to source DC continuous current @ T_{case}=25°C	30	A
5	$I_{ds\text{-}max}$	Drain to source pulse current @ T_{case}=25°C, pulse width 10 µs, V_{GS} = 6 V	45	A
6	$I_{ds\text{-}max}$	Drain to source DC current @ T_{case}=100°C	22	A
7	$dv/dt_{\text{-}max}$	Drain to source voltage slew rate	150	V/ns
8	$T_{J\text{-}max}$	Max junction temperature	150	°C
9	$T_{S\text{-}storage}$	Storage temperature	-55 to 150	°C

Thermal and Soldering Characteristics (Typical)

	Symbols	Parameters	Value	Unit
1	R_{thJC}	Thermal resistance (junction to case)	0.9	°C /W
2	R_{thJA}	Thermal resistance (junction to ambient)	62	°C /W
3	T_{solder}	Reflow soldering temperature	260	°C

Ordering

Order Code	Package Type	Packaging Method	Qty
GPIXU30SB5L	TO263-5L		

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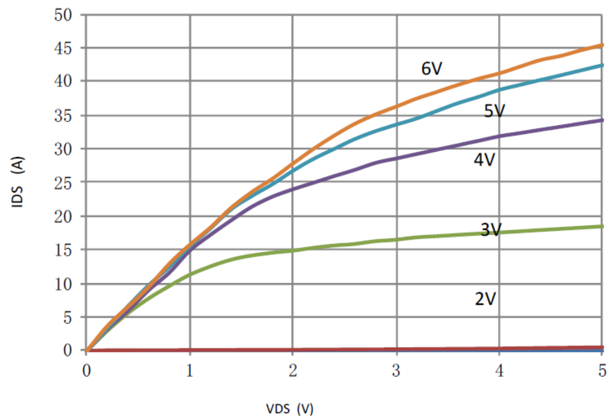
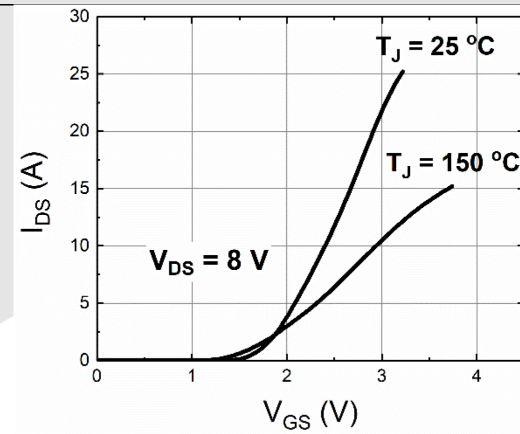
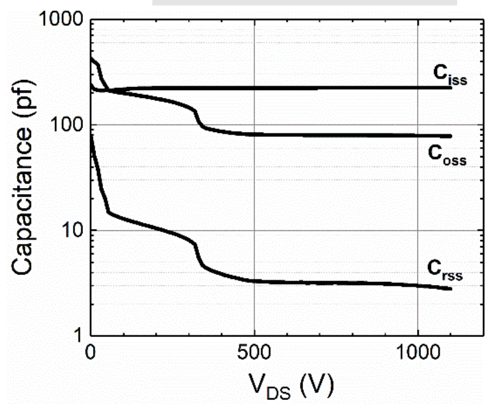
Electrical Performance



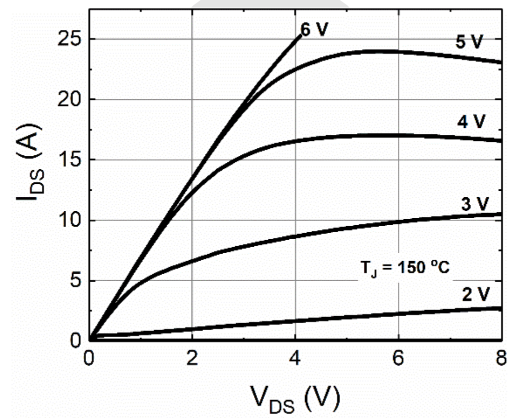
I_{DS} vs. V_{DS} @ T_j = 25 °C



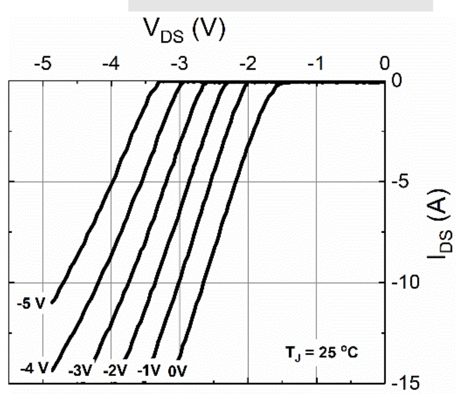
I_{DS} vs. V_{GS} @ T_j = 25 °C and 150 °C



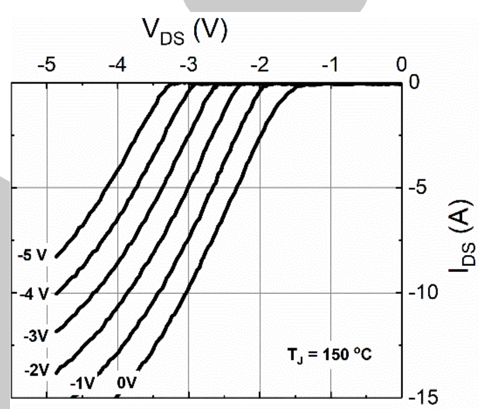
Capacitance vs. V_{ds} Curve @ T_j =25 °C



I_{DS} vs. V_{DS} @ T_j = 150 °C



Isd vs. Vsd reverse conduction curve @ T_j = 25 °C



Isd vs. Vsd reverse conduction curve @ T_j = 150°C

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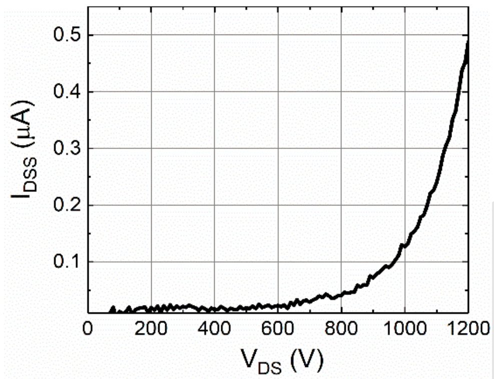
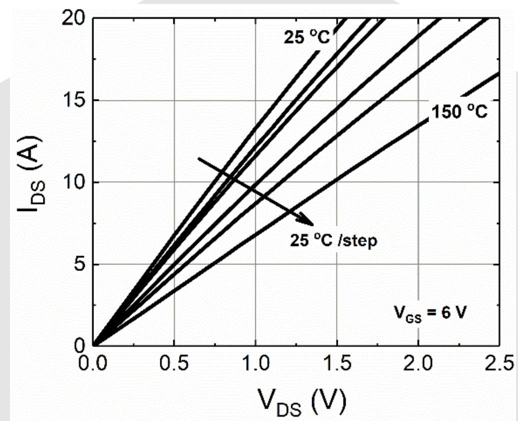
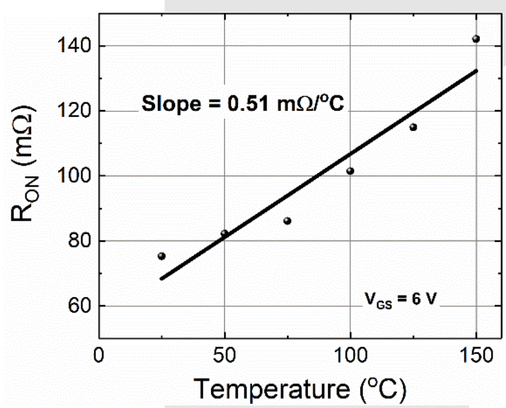


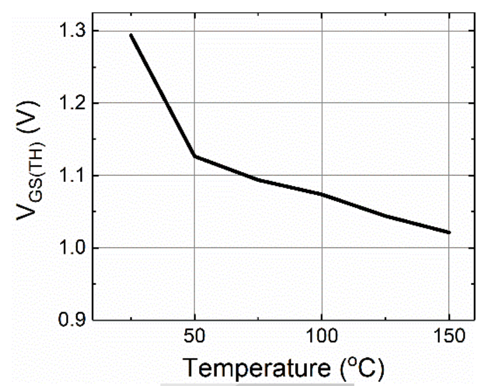
Typical off-state drain leakage current I_{DSS} vs. V_{DS} @ T_J = 25 °C



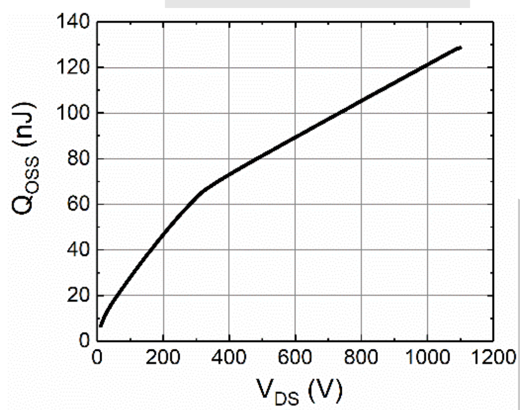
I_{DS} vs. V_{DS} @ V_{GS} = 6V, T_J=25-150 °C



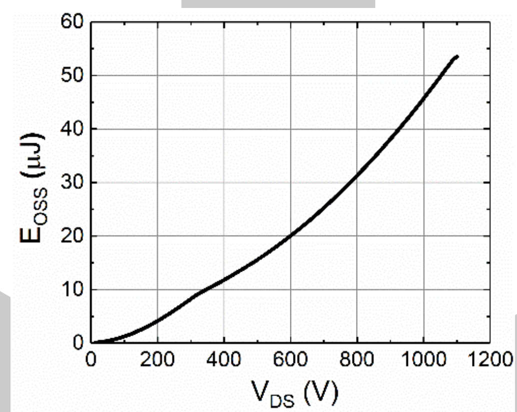
On-state resistance vs. T_J @ I_D = 7.5 A, V_{GS} = 6V



Typical $V_{GS(TH)}$ temperature dependence $V_{GS(TH)}$ vs. T_J @ V_{GS}=V_{DS}, I_D = 3.5 mA



Output charge Q_{OSS} vs. V_{DS}



Stored Energy Characteristic E_{OSS} vs. V_{DS}

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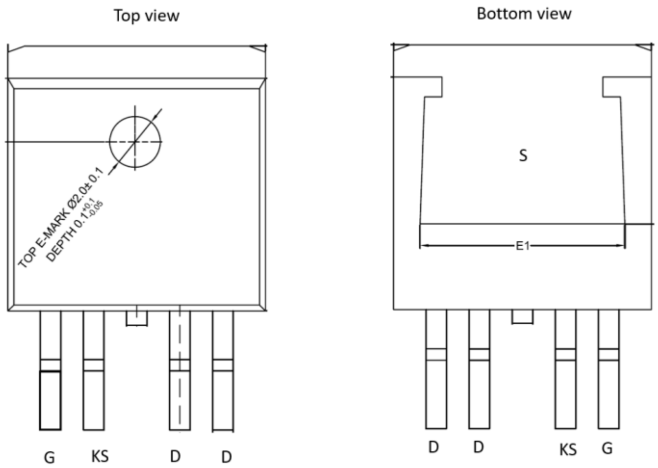
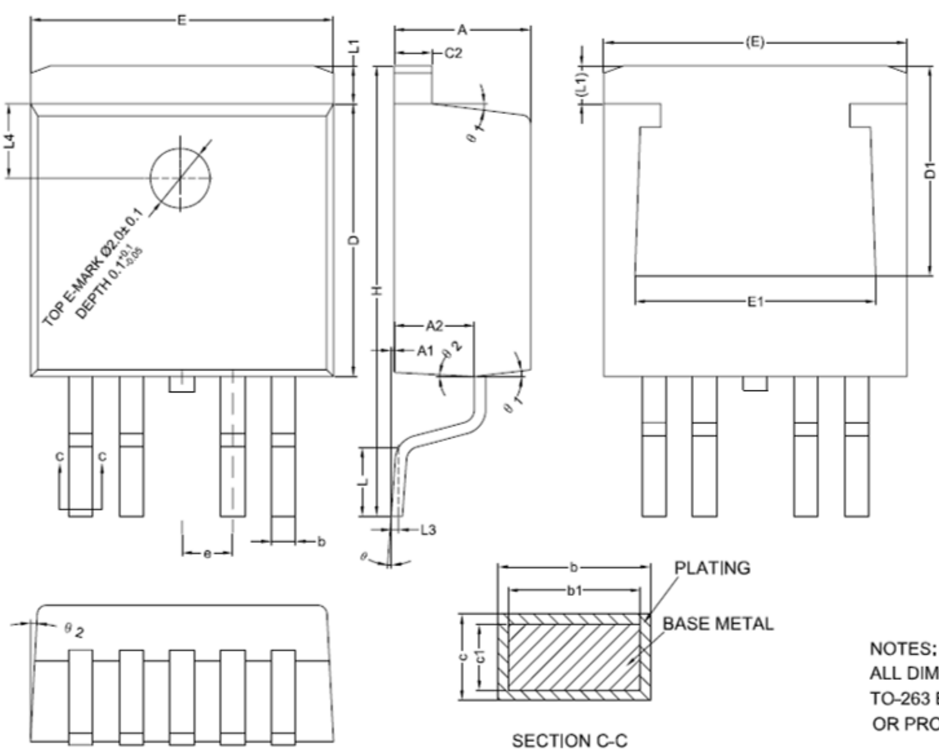
Package Information



Device code: GPIHVSB5L



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	4,40	4.57	4,70
A1	0	0,10	0.25
A2	2.59	2,69	2.79
b	0,77	-	0,90
b1	0,76	0.81	0,86
c	0,34	-	0,47
c1	0.33	0,38	0.43
c2	1.22	-	1.32
D	9,05	9.15	9,25
D1	6,86	-	7,50
E	10.06	10.16	10.26
E1	7.50	-	8.30
e		1.70BSC	
H	14.70	15.10	15.50
L	2.00	2.30	2,60
L1	1,17	1,27	1,40
L3		0,25BSC	
L4		2.00REF	
θ	0°	-	8°
θ 1	5°	7°	9°
θ 2	1°	3°	5°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-263 BA DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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GaN HEMT Frequently Asked Questions

1	Q: Can we do pin to pin switch for silicon MOSFET or IGBT? A: The short answer is no. GaN HEMT power devices are far superior than the best silicon devices such as super junction MOSFETs. However, due to different requirements of gate driving voltage and extremely high dv/dt slew rate, special drivers and optimized PCB layouts are recommended to minimize the impact from circuit parasitics. For the packaging form in **TO-263-5**, the middle pin is recommended to seal with insulating glue on PCB board to prevent arcing.
2	Q: How do GaN power devices compare with SiC? A: Currently GaN power HEMT devices are most suitable for low to medium voltage (≤1200V) and power (<20KW) applications. GaN is the ideal choice for high frequency applications. SiC devices are better choice for high voltage and high-power applications (>20KW).
3	Q: Do we need to parallel an FRD for applications such as inverters? A: GaN devices are different from silicon MOSFET or IGBT in that they have no inherent PN junction diodes that cause reverse recovery issue. User do not need to parallel an FRD for the purpose of suppressing the body diode reverse recovery effect, since GaN HEMT can operate in both first and third quadrants. However, care should be taken for the dead time power loss since the Vsd voltage of GaN HEMT is usually close to 2V. This is especially true when a negative gate voltage is applied.
4	Q: Can we parallel GaN HEMT devices? A: Yes, GaN HEMT is ideal for paralleling, due to the positive temperature coefficient of $R_{ds,on}$. Hence, paralleling GaN HEMT devices are encouraged.